

Amendments to the Claims

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Claims 1-20 (Canceled).

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21. (Currently Amended): DRAM circuitry comprising:  
an array of word lines forming gates of field effect transistors and an array  
of bit lines, individual field effect transistors comprising a pair of source/drain  
regions; and  
a plurality of memory cell storage capacitors associated with the field  
effect transistors, individual storage capacitors comprising a first capacitor  
electrode in electrical connection with one of a pair of source/drain regions of  
one of the field effect transistors and a second capacitor electrode, a capacitor  
dielectric region received intermediate and contacting each of the first and  
second capacitor electrodes, the capacitor dielectric region having a thickness  
less than or equal to 60 Angstroms and comprising aluminum nitride, the other of  
the pair of source/drain regions of the one field effect transistor being in  
electrical connection with one of the bit lines.

22. (Currently Amended): The circuitry of claim 21 wherein the  
capacitor dielectric region contacts each of the first and second capacitor  
electrodes and consists essentially of aluminum nitride.

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cont.*

23. (Currently Amended): The circuitry of claim 21 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes and consists essentially of aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

Claim 24 (Canceled).

25. (Currently Amended): The circuitry of claim 21 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

Claims 26 and 27 (Canceled).

28. (Previously Presented): The circuitry of claim 21 wherein the aluminum nitride is substantially amorphous.

Claims 29-64 (Canceled).

65. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes and consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

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Claim 66 (Canceled).

67. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes and has a thickness less than or equal to 50 Angstroms.

68. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride, and has a thickness less than or equal to 60 Angstroms.

Claim 69 (Canceled).

70. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

71. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region contacts each of the first and second capacitor electrodes, consists essentially of substantially amorphous aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

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Claims 72 and 73 (Canceled).

74. (Previously Presented): The circuitry of claim 21 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

75. (Previously Presented): The circuitry of claim 28 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

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